

#### REMARKS

1. Claims 1-13 have been cancelled and replaced with new claims 14-68.
2. Claims 14-68 have been added to replace previously pending claims 1-13. The new claims address and overcome the rejection of claim 2 under 35 U.S.C. §112, first paragraph, and claims 9 and 11 under 35 U.S.C. §112, second paragraph.
3. New claims 14-68 are not unpatentable over Watanabe in view of Lane.

The solution disclosed in Watanabe is essentially different than that of the present invention. Watanabe et al. (US 6,310, 897) discloses an information transmission method wherein a transmission side transmits reconstruction information required to reconstruct contents of header information or part of the header information upon adding the reconstruction information to encoded information. Furthermore, the reception side performs an error check with respect to the header information or part of the header information and decodes the encoded information by using the reconstruction information as a substitute when an error is detected by the error check. In short, Watanabe relates to error detection and error correction applied to multiplexed signals (performed by adding redundant e.g. header information).

In Watanabe, designation information is inserted in the bit stream before the transmission (see e.g. abstract, col. 2, lines 55-65). In Applicants' invention, the error type indication

that is forwarded to the video decoder is a result of "detecting at multiplexing" a possible invalidity of a demultiplexed video data unit. The received multiplex signal is demultiplexed. Furthermore, the purpose of Watanabe is to ensure reconstruction of header information (at the receiving end) even if an error is introduced in the bit stream. Watanabe does not disclose the fact that error type indication is forwarded to the video decoder as recited in the claims.

The Office Action states that Lane discloses adding an error indication to the demultiplexed video data signal. Lane indeed discloses a step in which an error indicator signal is inserted into the first byte of a processed packet (e.g. col. 7, lines 20-19). Lane describes that if a packet is error free the inserted byte is 47 HEX, which is equivalent to the value of the sync byte. If the packet contains error(s), the inserted byte differs from the 47 HEX value.

Lane (US 5,956, 102) discloses methods and apparatus for performing packet synchronisation recovery and error detection operation on packets including a CRC check byte. Lane describes a CRC decoder circuit operating to perform both packet synchronisation and error checking operating in one of two modes: 1) a packet sync acquisition mode or 2) a sync locked mode of operation. Lane describes also a feature in which an error indicator can be inserted in a packet. If a packet is erred, the CRC syndrome byte is inserted into the corresponding packet used to produce a syndrome byte. Therefore, the syndrome byte is packet error indicator. However, when the packet is error free, the first byte of the packet will have the expected 47 HEX sync byte value. In short, Lane discloses adding an error indication to data extracted from a transport packet.

In Lane the inserted byte comprises only an error indication, that is, the inserted byte merely indicates that the packet contains an error. The solution described in Lane does not disclose any further information about the indicated error. Furthermore, the error indication is in every erroneous packet (the first byte). In the present invention, error type indication in the described embodiments may be supplemented with further information about the error (e.g. error location etc.). Therefore, in Lane there might arise a situation in which retransmission of a packet is necessary because the first byte of a packet indicated an error. According to the solution described in the present invention, retransmission may not be needed at all because the aforementioned error type and possible further information about the error can enable a video decoder to take appropriate action to conceal the effects of the error.

It is submitted that it would not have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the method of adding an error indication to an error data packet disclosed by Lane into the Watanabe system. In order to establish a *prima facie* case of obviousness there be some motivation, recited in the references, to combine the references in the manner proposed. (See M.P.E.P. §2173 et seq.) It is submitted that neither reference provides any such motivation.

First, the solution disclosed in Lane does not mention multiplexing and/or demultiplexing at all. Secondly, Watanabe does not suggest, teach or motivate in any way that the solution disclosed in Lane could be combined to the solution disclosed in Watanabe. Therefore, there is no motivation to combine the two

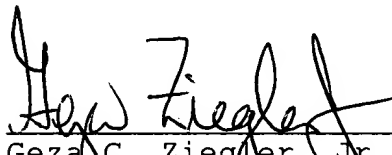
references, and the combination does not achieve Applicants' invention, or disclose or suggest each element of Applicants' invention as required under 35 U.S.C. §103(a).

As a summary, Watanabe in view of Lane does not disclose the present invention. Furthermore, there is no motivation to combine the solution disclosed in Lane with the solution disclosed in Watanabe.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record, and are in proper form for allowance. Accordingly, favorable reconsideration and allowance is respectfully requested. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

A check in the amount of \$1,550.00 is enclosed for the additional claims fee and a three-month extension of time. The Commissioner is hereby authorized to charge payment for any fees associated with this communication or credit any over payment to Deposit Account No. 16-1350.

Respectfully submitted,

  
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